CLASS-DE POWER AMPLIFIERS WITH RESISTIVE LOAD

Anton S. Alipov (*Associate Member*, IEEE), Vladimir A. Sokolov, and Viktor B. Kozyrev

Moscow Technical University of Communications and Informatics,
8a Aviamotornaya, Moscow, 111024, Russia

***Abstract* — New class-DE switched-mode power amplifiers with resistive load (which is practically realized as a diplexer) are proposed and analyzed. Two possible types of such amplifiers – with an L-type shaping circuit and with a parallel one – are considered. It is shown that the power of higher harmonics at the input of the diplexer considerably lowers with increasing the deadtime intervals in class-DE operation, and, consequently, the dc-to-fundamental conversion efficiency of these amplifiers approaches that of the class-DE amplifiers with resonant load.**

***Index Terms* — HF amplifiers, inverters, power amplifiers, switching amplifiers, radio transmitters.**

I. Introduction

Nowadays a growing interest to class-DE power amplifiers [1 – 4], invented as far back as 1975 [5], is observed. These switched-mode amplifiers essentially present an extension of voltage-mode class-D amplifiers with resonant load [6, 7]. As compared to the latter, class-DE amplifiers are free from the switching power losses associated with the transistor output capacitances. To achieve this goal transistors operate with deadtimes, during which their output capacitances are recharged, and a supplementary inductance is added either in series [1 – 3, 5] or in parallel [4] with the resonant load. Together with the total output capacitance this inductance forms an L-type or a parallel circuit respectively. The transient that takes place in this circuit during the deadtimes determines the shape of the drain-to-source (ds) voltage. Therefore, by analogy to class-E amplifiers, this circuit is termed "shaping circuit (SC)" [4].

On the other hand, switching power losses are also inherent to class-D amplifiers with resistive load [6, 7] (both voltage-mode and current-mode). When it is required to obtain the fundamental current in the load, such amplifiers are terminated with a diplexer. The power of the fundamental is then delivered to the main load at the output of the low-pass filter, and the power of the higher harmonics is dissipated in the ballast at the output of the high-pass filter. The diplexer is designed so that its input impedance was (ideally) constant and resistive at all frequencies, as if the amplifier was terminated with a resistor simply (hence the term "resistive load"). The advantages of class-D amplifiers with resistive load over those with resonant one are lower crest-factors of either drain voltage or current and better tolerance to load mismatches [6, 7]. The principal disadvantage, which substantially restricts their usage, is relatively low dc-to-fundamental conversion efficiency (η_1), the cause being that considerable power of higher harmonics is wasted in the ballast. If each of two transistors is on for the half-cycle (rectangular drain waveforms), η_1 is only 0.81 (even assuming that no switching losses are present). By shifting from rectangular waveforms η_1 can be raised up to 0.92, but the transistor utilization factor lowers in this case [7].

Through simulation we observed that the voltage-mode class-D amplifier with resistive load can as well operate in the class-DE mode. As in the class-DE amplifiers with resonant load, deadtimes are to be introduced and a supplementary inductance is to be added, either in series or in parallel with the resistive load. Such a solution has the following practical value. As the deadtime interval is increased from 0 to 180°, the input current of the diplexer transforms from rectangular to sinusoidal, that is η_1 grows from 0.81 to 1 theoretically. Therefore it is reasonable to expect that under the practical deadtime values of up to 90° the dc-to-fundamental conversion efficiency of *class-DE* amplifiers with *resistive* load may considerably exceed the efficiency of *class-D* voltage-mode amplifiers with *resonant* load (because the switching losses are excluded) and approach that of *class-DE* amplifiers with *resonant* load, whereas the advantages of the resistive load over the resonant one are maintained as well.

In this paper the analysis of the proposed amplifiers is performed, and efficiency comparison between three types of amplifiers – class-DE with resistive load, class-DE with resonant load, and class-D with resonant load – is carried out. As the analysis procedures for the amplifiers with an L-type SC and with a parallel SC are essentially similar, only the analysis of the former amplifier is presented in detail, and for the latter one the corresponding results are only given, mainly in graphic form.

II. Current And Voltage Waveforms

The equivalent circuits of class-DE amplifiers with resistive load (considered here a simple resistor) and two types of SC are shown in Fig. 1,a and Fig. 1,b respectively. C_Σ is the total output capacitance of two

transistors (switches) and L is the SC inductance. According to Fig. 1, the voltage across S1 is V_{ds}, and that across S2 is $V_{DC} - V_{ds}$, where V_{DC} is the supply voltage. If the state of the circuit is steady, the voltages across the blocking capacitors C_{b1} and C_{b2} are $V_{DC}/2$.

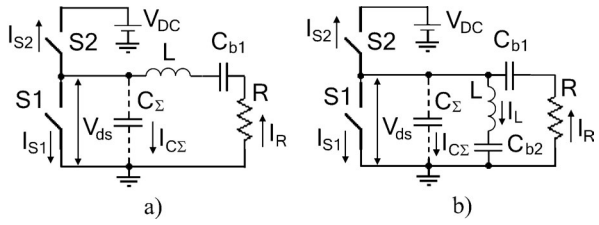

Fig. 1: Equivalent circuits of class-DE amplifiers with resistive load: a) – with an L-type SC, b) – with a parallel SC.

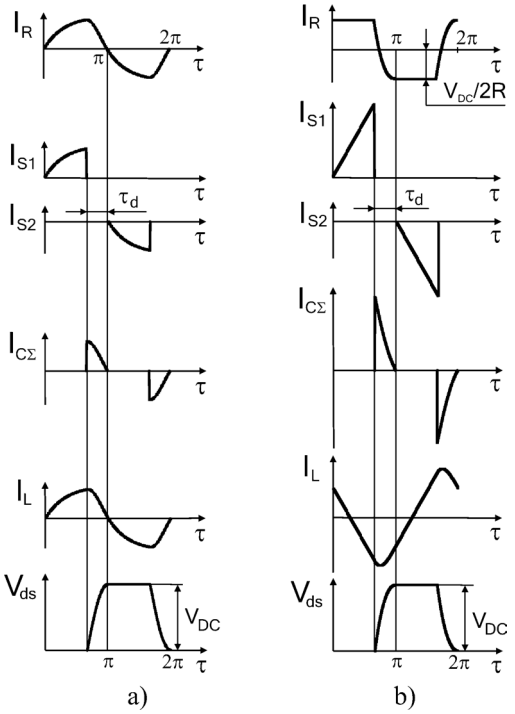

Fig. 2: Waveforms in class-DE amplifiers with resistive load: a) – with an L-type SC, b) – with a parallel SC.

The waveforms for the two amplifiers are shown in Fig. 2,a and Fig. 2,b respectively. When deriving them, it is sufficient to consider only half of the cycle, i. e. the interval $0 < \tau < \pi$, where $\tau = 2\pi ft$, and f is the fundamental frequency. Indeed, due to the symmetry of the circuit the analytical expressions of the waveforms on the interval $\pi < \tau < 2\pi$ can be found as

$$V_{ds}(\tau) = V_{DC} - V^*_{ds}(\tau - \pi);\ \ I(\tau) = -I^*(\tau - \pi),$$

where the index "*" marks the corresponding dependences on the interval $0 < \tau < \pi$, and I(...) stands for the currents of either switch, of the total output capacitance, of the load resistance, and of the supplementary inductance. The analysis of the waveforms in the amplifier with an L-type SC is conducted as follows.

During the interval $0 < \tau \le \pi - \tau_d$, where τ_d is the deadtime in angular measure (see Fig. 2), switch S1 in Fig. 1,a is short circuited, and switch S2 is open circuited: $I_{S2} = 0$, $I_{C\Sigma} = 0$, $V_{ds} = 0$. It is easily shown that

$$I_{S1} = I_R = \frac{V_{DC}}{2R}\left(1 - e^{-\frac{\tau}{l}}\right),$$

where $l = 2\pi fL/R$. During the interval $\pi - \tau_d < \tau \le \pi$ both switches are open circuited: $I_{S1} = 0$, $I_{S2} = 0$, $I_{C\Sigma} = I_R$. The transient in the network is described by the differential equation

$$\frac{d^2 I_R}{d\tau^2} + \frac{R}{2\pi fL}\frac{dI_R}{d\tau} + \frac{1}{4\pi^2 f^2 LC_\Sigma} I_R = 0.$$

Solving it with the initial conditions $I_R(\pi - \tau_d) = I_{S1}(\pi - \tau_d)$, $V_{ds}(\pi - \tau_d) = 0$, we obtain

$$I_R = I_{C\Sigma} = \frac{V_{DC}}{2R} e^{-\frac{\tau}{2l}} (G\cos(\beta\tau) + H\sin(\beta\tau)), \quad (1)$$

$$V_{ds} = \frac{V_{DC}}{2}\left[1 - e^{-\frac{\tau}{2l}}\left[\left(\frac{G}{2l} + H\beta\right)\cos(\beta\tau) + \left(\frac{H}{2l} - G\beta\right)\sin(\beta\tau)\right]\right], \quad (2)$$

where

$$G = 2sh\left(\frac{\tau_o}{2l}\right)\cos(\beta\tau_o) - \frac{1}{\beta l} ch\left(\frac{\tau_o}{2l}\right)\sin(\beta\tau_o),$$

$$H = 2sh\left(\frac{\tau_o}{2l}\right)\sin(\beta\tau_o) + \frac{1}{\beta l} ch\left(\frac{\tau_o}{2l}\right)\cos(\beta\tau_o),$$

$$\beta = \frac{1}{2l}\sqrt{\left(\frac{2l}{c} - 1\right)}, \quad c = \pi fC_\Sigma R, \quad \tau_o = \pi - \tau_d.$$

The obtained expressions of the waveforms include undetermined parameters c, l, and τ_d. Under the fixed deadtime τ_d two normalized SC parameters – c and l – remain unknown. To find them in function of the deadtime, the class-DE switching conditions [1 – 5] are to be used: $V_{ds}(\pi) = V_{DC}$, $I_{C\Sigma}(\pi) = 0$. Equalizing the right sides of (2) and (1) to V_{DC} and to 0 respectively and substituting π for τ, we get a set of two equations, from which the dependences $c(\tau_d)$ and $l(\tau_d)$ can be derived (see Fig. 3).

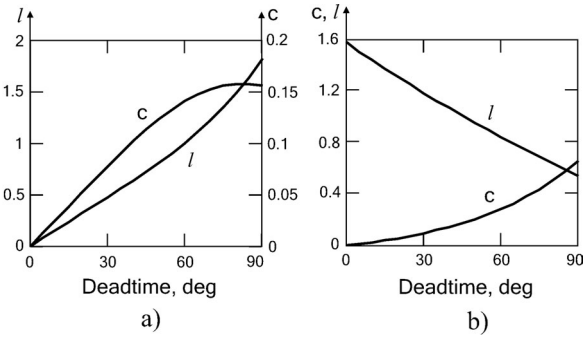

Fig. 3: Normalized parameters of the elements of the L-type (a) and of the parallel (b) SC in function of the deadtime τ_d.

III. Parameters Of The State

The state of amplifier's output network is described by the waveform expressions obtained in Section II. Yet for the design of the amplifier it is convenient to know some integral parameters of the state. One such parameter is the ratio ξ between the power P_1 of the first harmonic in the resistance R (or the power delivered to the main load of a practical amplifier) and the total power P_R dissipated in this resistance (or the total power delivered to the main and ballast loads of the diplexer). The power balance equation for the circuits of Fig. 1 is

$$P_0 = I_{d0}V_{DC} = P_R = P_1/\xi = \\ = \frac{I_d^{(1)}V_{ds}^{(1)}\cos(\arg \dot{I}_d^{(1)} - \arg \dot{V}_{ds}^{(1)})}{\xi}, \qquad (3)$$

where P_0 is the power consumed from the supply, I_{d0} is the dc component of the drain current, $\dot{I}_d^{(1)}$ and $\dot{V}_{ds}^{(1)}$ are the first harmonics of the drain current and the ds voltage, $I^{(1)}_d$ and $V^{(1)}_{ds}$ – the corresponding magnitudes.

The drain current of a transistor comprises the switch current and the current of the transistor's output capacitance. Since the latter current does not contain a dc component, I_{d0} is determined solely by the I_{S1} (or I_{S2}) waveform. Further, the first harmonic of $I_{C\Sigma}$ and hence the first harmonic of the current of the transistor's output capacitance are orthogonal to $\dot{V}_{ds}^{(1)}$ (for V_{ds} is the voltage across C_Σ). Therefore

$$I_d^{(1)}\cos(\arg \dot{I}_d^{(1)} - \arg \dot{V}_{ds}^{(1)}) = I_S^{(1)}\cos(\arg \dot{I}_S^{(1)} - \arg \dot{V}_{ds}^{(1)}),$$

where $\dot{I}_S^{(1)}$ is the first harmonic of the switch current and $I^{(1)}_S$ – its magnitude. Consequently

$$\xi = \frac{P_1}{P_R} = \frac{I_S^{(1)}V_{ds}^{(1)}\cos(\arg \dot{I}_S^{(1)} - \arg \dot{V}_{ds}^{(1)})}{I_{d0}V_{DC}}.$$

I_{d0}, $\dot{I}_S^{(1)}$ and $\dot{V}_{ds}^{(1)}$ are found from the Fourier decomposition of the waveforms derived in Section II. The dependences of ξ on τ_d are shown in Fig. 4. As the deadtime interval is increased, ξ rapidly grows from $8/\pi^2$ at $\tau_d = 0$ (which corresponds to rectangular drain waveforms, i. e. pure class-D) and approaches unit (sinusoidal waveforms).

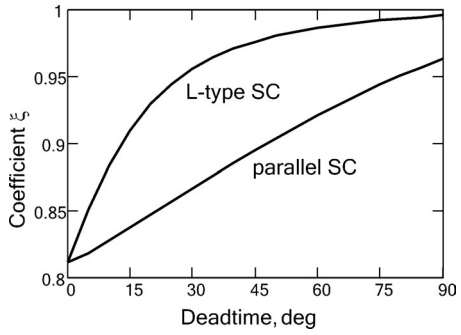

Fig. 4: Dependences of ξ on the deadtime τ_d

For the design of the amplifier it is also necessary to know the relationship between the required deadtime and the parameters set on design, i.e. f, P_1, V_{DC}, C_Σ.

Having derived I_{d0}, from (3) for the amplifier with an L-type SC we obtain

$$\frac{2\pi f C_\Sigma V_{DC}^2}{P_1} = \frac{8\pi c}{\xi}\left[\pi - \tau_d + l\left(e^{\left(\frac{\tau_d - \pi}{l}\right)} - 1\right)\right]^{-1}. \qquad (4)$$

As follows from Fig. 1,b, in the amplifier with a parallel SC $P_1 = [V^{(1)}_{ds}]^2/2R$, hence

$$\frac{2\pi f C_\Sigma V_{DC}^2}{P_1} = 4c\left(\frac{V_{DC}}{V_{ds}^{(1)}}\right)^2. \qquad (5)$$

The right sides of (4) and (5) depend on τ_d solely, since c, l, ξ, and $V^{(1)}_{ds}/V_{DC}$ are functions of τ_d. The dependences of τ_d on $2\pi f C_\Sigma V^2_{DC}/P_1$ for the two amplifiers coincide approximately.

IV. Efficiency Of The Output Network

To determine the efficiency of amplifier's output network one should consider not only the power loss of the higher harmonics (characterized by the coefficient ξ), but also the power losses in the transistors and in the SC inductor. The power loss in a turned on transistor is associated with the drain, source and channel parasitic resistances. Further, power is also wasted in the transistors when they are off, since cur-

rent is flowing through their output capacitances and, hence, through the parasitic drain and source resistances. These losses can be calculated after deriving the RMS currents of an on transistor (i. e. the RMS switch current), of an off transistor (i.e. the RMS value of $I_{C\Sigma}/2$), and of the SC inductor (the RMS value of I_R in the case of the L-type SC). RMS currents are found by using the waveform expressions from Section II. The dc-to-fundamental conversion efficiency is then $\eta_1 \approx P_1/(P_1/\xi + P_{dis})$, where P_{dis} is the total power loss in the transistors and the SC inductor.

To simplify the efficiency comparison between different amplifiers we assumed that no power is wasted in the SC inductor, and that the parasitic resistance of an on transistor is equal to that of an off one (i. e. the channel resistance is negligible). Fig. 5 shows the calculated dependencies of η_1 on $2\pi fC_\Sigma V^2_{DC}/P_1$ with $\varepsilon \equiv rP_1/V^2_{DC}$ as a parameter (r is the total parasitic resistance of a transistor). If C_Σ, V_{DC}, and P_1 are given, these curves present the dependences of η_1 on the operating frequency.

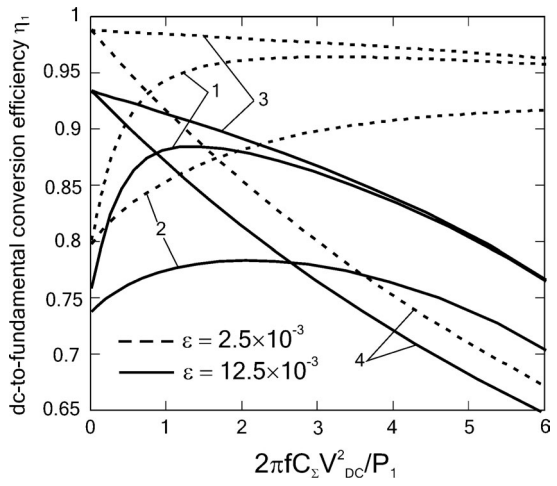

Fig. 5: Dependences of η_1 on $2\pi fC_\Sigma V^2_{DC}/P_1$ for class-DE amplifiers with resistive load and an L-type SC (1), with resistive load and a parallel SC (2), with resonant load (3), and for a voltage-mode class-D amplifier with resonant load (4).

The efficiency dependences for class-DE amplifiers with resonant load (coinciding for two types of SC), calculated in a similar way, were taken from [4]. The dependences for a class-D voltage-mode amplifier with resonant load were calculated in assumption that the switching power loss associated with the output capacitances equals $fC_\Sigma V^2_{DC}$ [6].

From Fig. 5 three important conclusions follow. Firstly, since the switching power loss is absent, at relatively high values of $2\pi fC_\Sigma V^2_{DC}/P_1$ the efficiency of class-DE amplifiers with resistive load considerably exceeds that of a voltage-mode class-D amplifier with resonant load. Secondly, with raising $2\pi fC_\Sigma V^2_{DC}/P_1$ the efficiency of class-DE amplifiers with resistive load tends to approach the efficiency of class-DE amplifiers with resonant load. Indeed, higher values of $2\pi fC_\Sigma V^2_{DC}/P_1$ require larger deadtime intervals, and the larger τ_d, the lower the level of the higher harmonics at the input of the diplexer, i. e. the closer dc-to-fundamental conversion efficiency to dc-to-RF conversion efficiency. Lastly, the comparison between two class-DE amplifiers with resistive load shows that the amplifier utilizing a parallel SC has considerably lower η_1 than the one with an L-type SC. That is caused by the highly peaked switch current waveform (see Fig. 2,b). From Fig. 5 it is obvious that only the amplifier with an L-type SC is competitive with class-DE amplifiers with resonant load in terms of efficiency.

V. Conclusion

New class-DE power amplifiers with resistive load have been proposed and analyzed, and the parameters necessary for the design have been derived. The amplifier with an L-type SC proves to be competitive with class-DE amplifiers with resonant load in terms of efficiency. Whether the introduced amplifiers maintain the advantages of class-D amplifiers with resistive load (e. g. good tolerance to load mismatches) is a question of further investigation.

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